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EXAMINER	
WONG, LINDA	

ART UNIT	PAPER NUMBER
2634	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,253	GLENN ET AL.	
	Examiner	Art Unit	
	Linda Wong	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-9,11,13,17,18,20-24,26-28 and 30* is/are rejected.

7)☒ Claim(s) *4,10,12,14-16,19,25 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "150" and "240" have both been used to designate a Highly Linear Phase Interpolator. There are other similar components in the diagrams that should have the same reference characters.

2. The drawings are objected to because

   a. In Fig. 1, the output of the highly linear phase interpolator is inputted into the phase controller. In Fig. 2, the output of the phase controller is inputted into the highly linear phase interpolator. The same is found in Fig. 8.

   b. In Fig. 1, the input to the phase-frequency detector is a conditioned-data signal, which is different from the data signal received by the receiver front end. In Fig. 2, the input to the phase-frequency detector is a labeled as a data signal, not a conditioned-data signal.

   c. Inputs and outputs to each component found in Figures 1, 2, 5 and 8 should be added to the diagrams to clarify the association of the components.

   d. In Fig. 1, the phase controller outputs control signal(s) to the phase update logic and receive trip signal(s) from the phase update logic. In Fig. 2, the phase update logic inputs control signal(s) to the phase controller and the trip signal(s) are not shown.

   e. In Fig. 2, output and input arrows used to indicate inputs and outputs are necessary for the components in label 240.

f. In Fig. 5, the interrelated control signal and overflow or trip signals are outputted from the phase controller. In Fig. 1, both of these signals are inputs to the phase controller.

g. In Fig. 5, the label for the entire apparatus is voltage controller. It is suggested that this label be changed to phase controller.

h. In Fig. 6, the labels VC A and VC B are not shown in Fig. 5. Also, the output labels 660 and 670 should also be shown in Fig. 5.

i. In Fig. 8, inputs and outputs to/from each component should be clearly shown in the diagram.

j. Consistent labels to components. Phase control circuitry is mentioned in the Fig. 2 and 8 and claim 1. By having similar terminology, when matching with specifications, it is hard to determine which reference is being used in claim 1. Please change the written labels similar in figures 2 and 8. For example, phase controller in fig 2 should be changed to voltage controller to match the label found in fig. 8. also page 6, paragraph [0049], line 6 and paragraph [0053], line 8 the term phase controller should be changed if changes are made in Fig. 2.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. **Claims 5 and 6** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. **Claim 5** recites a degenerative mesh circuitry coupled to a first and second circuitry of the phase control circuit. Claim 5 also cites the degenerative mesh circuit degenerates an amplifier comprising a first, second and degenerative mesh circuitry, which indicates that the amplifier comprises all three types of circuitry. The recitations in claim 5 do not clearly state where the degenerative mesh circuitry lies. Is the degenerative mesh circuitry coupled between the first and second circuitry found in the phase control circuit? Or is the degenerative mesh circuitry part of an amplifier comprising all three types of circuitry? According to the specification, the degenerative mesh circuitry is interconnected to the phase control circuitry, which does not indicate the mesh circuitry is connected between the first and second circuitry found in the phase control circuitry as recited in the claim. (page 12, paragraph [0092], lines 1-2) Furthermore, Figure 8 shows the degenerative mesh between the phase control circuitry and the current mirror circuit, all part of the control current circuitry, which is

different from the phase control circuitry as recited in the independent claim 1. (Fig. 8, labels 814, 850 and 812)

4. **Claim 6** recites "substantially equivalent impedances coupled between more than 2 circuits of said phase control circuitry." In the specification, the degenerative mesh circuitry comprises such a limitation, but as the rejection to claim 5 describes the discrepancy of the location of the degenerative mesh, such a rejection is valid to claim 6. Is the degenerative mesh, where the impedances are substantially equivalent, lie within the phase control circuitry as recited in the claim or between two circuits found in the current control circuitry as show in Fig. 8?

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claim 5** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 5 recites the limitation "degenerative mesh circuitry coupled ... to degenerate an amplifier comprising the first circuit, second circuit, and the degenerative mesh." This limitation is unclear and indefinite. Is the first and second circuitry part of the amplifier as indicated by the phrase "the amplifier comprising .."? Is the first and second circuitry part of the phase control circuitry as indicated by the phrase "degenerative mesh circuitry coupled between a first circuitry of said phase control circuitry and a second circuit of said phase control circuitry"?

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1,2,3,7-9,11** are rejected under 35 U.S.C. 102(e) as being unpatentable by Chao et al (US Patent No.: 6380783).

   a. **Claim 1**, Chao et al discloses a interpolator circuitry using a weighted bias current to adjust the clock phases, a phase control circuit for adjusting the phases based on a controlled signal and an output circuitry for outputting a phase based on the adjusted clock phases. (Fig. 1, labels 12, 24, 16, 18 and 22) Although Chao et al does not explicitly state adjusting amplitude of the clock phases, the bias current generator produced weighted bias currents, which regulate the phase interpolator. Thus it would be obvious to one skilled in the art that the amplitude of the clock phases would be adjusted based on the bias currents.

   b. **Claims 2 and 3**, Chao et al discloses a weighted bias generator, which provides a static bias current as well as controlling the bias current fed coupled to the phase control circuitry. (Fig. 1, labels 16 and 12)

   c. **Claims 7**, Chao et al discloses an interpolator comprising a current-steering mechanism for adjusting the current based on the bias current generated. (Fig. 5A, and Col. 5, lines 18-67 and Col. 6, lines 1-19)

d. **Claim 8,** Chao et al discloses steering the current between two conductive paths. (Figures 5 and 5A and Col. 5, liens 18-65)

e. **Claim 9**, Chao et al discloses an interpolator comprising a current-steering mechanism wherein the weighted bias currents adjust the clock phases. Since the bias currents are weighted and the clock phases are adjusted based on these bias currents, it would obvious to one skilled in the art that the amplitude of the bias currents affect the adjustments of the amplitude of the clock phases. (Fig. 5A, Col. 5, lines 18-67 and Col. 6, lines 1-19)

f. **Claim 11**, Chao et al discloses a connection between the weighted bias current and the current steering mechanism or phase interpolator (Fig. 1, labels 16 and 18) Although Chao et al does not explicitly state a conductive path coupled between the current source and current-steering mechanism, in order to produce a current to the phase interpolator, it is inherent to use a conductive path.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 13,17,18,20-24,26-28,30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al (US Patent No.: 6380783) in view of Buchwald et al (US Patent No.: 6509773).

   a. **Claim 13,** Although Chao et al does not teach combining the first and second phases, Buchwald et al discloses combining a plurality of adjusted phases outputted. (Col. 2, lines 26-28, Fig. 9, labels 804 and 826 and Col. 15, lines 35 and 39) It would be obvious to one skilled in the art to replace the comparator found in Chao et al with the combiner found in Buchwald et al to provide adjusted phase based on multiple changes to effectively sample high data rate signals to reduce cost, size and power dissipation.

   b. **Claim 17** inherits all the limitations of claims 1 and 13.

   c. **Claim 18** inherits all the limitations of claim 13.

   d. **Claim 20**, Chao et al discloses receiving more than 1 phase of a reference clock signal (Fig. 1, labels 26,28,30 and 32), wherein the phases outputted to the selector found in Chao et al comprises two phases that are less than 180 degrees apart. (Col. 3, lines 54-59)

   e. **Claim 21**, Chao et al discloses receiving control signals, wherein the first and second control signal (Fig. 1, labels clk_a and clk_b) are used to control, along with the bias currents, IA and IB, the increase and decrease in charge. (Col. 5, lines 18-43) Although Chao et al does not explicitly discloses adjusting the amplitude, the bias currents, IA and IB, are weighted and used to control the adjustments along with the control signals, clk_a and clk_b. It is obvious to one

skilled in the art that the amplitude would adjusted when using a weighted bias current to adjust the charge.

f. **Claim 22**, Chao et al discloses increasing the charge, controlled by clk_a, clk_b, IA and IB, at the same rate as decreasing the charge. Although Chao et al does not explicitly disclose an increase and decrease at the same rate, in Figure 6, the charge is displayed. The amplitudes are show to increase and decrease at the same rate. (Fig. 6 and Col. 5, lines 43-65)

g. **Claim 23** inherits all the limitations of claim 13 but claim 13 does not recite the first and second phase are proportioned based upon the voltage of the interrelated control signals. Chao et al discloses control signals wherein the phase interpolator adjusts the phase based on the voltage of clk_a and clk_b. (Fig. 6, and Col. 5, lines 18-43)

h. **Claim 24** inherits all the limitations of claim 1, but claim 1 does not recite a phase controller and a clock circuitry. Chao et al discloses a phase control circuitry (Fig. 1, labels 12 and 14), wherein the control signals for controlling adjustments and reference clock signals are provided. (Fig. 1, labels 12, and 14)

i. **Claim 26** inherits all the limitations of claim 8.

j. **Claim 27** inherits all the limitations of claim 11.

k. **Claim 28** inherits all the limitations of claim 1 and 13.

l. **Claim 30** inherits all the limitations of claim 13 but claim 13 does not recite the first and second phase are proportioned based upon the voltage of the

interrelated control signals. Chao et al discloses control signals wherein the phase interpolator adjusts the phase based on the voltage of clk_a and clk_b. (Fig. 6, and Col. 5, lines 18-43)

Allowable Subject Matter

8. **Claims 4,10,12,14-16,19, 25, 29** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

   a. Saze et al (US Publication No.: 20020172304)

   b. Agazzi et al (US Publication No.: 20020012152)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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